UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,049	12/20/2001	Victor Tan Cher 'Khng	00-1117	5617

22823 7590 09/10/2004

STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,049	CHER 'KHNG ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 58-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29 and 58-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicant's election without traverse of Group I, drawn to claims 1-29 and 58-64 in the reply filed on 6-17-4 is acknowledged.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 21, 25 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following is a quotation of MPEP 2111.01 [R-1]:

> THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION
> While the ** claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below)>; MSM Investments Co. v. Carolwood Corp., 259 F.3d 1335, 1339-40, 59 USPQ2d 1856, 1859-60 (Fed. Cir. 2001). One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification. It is only when the specification provides definitions for terms appearing in the claims that the specification can be used in interpreting claim language. In re Vogel, 422 F.2d 438, 441, 164 USPQ 619, 622 (CCPA 1970).

In claims 5, 21, 25 and 29 the scope of the term "bismaleimide-trizine (BT)" is unclear because the term has no plain meaning, and it is not otherwise clearly defined in the disclosure.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

Claim 1-4, 6-12, 14-20, 22-24, 26-28 and 58-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Glenn (6586826).

At column 3, line 9 to column 6, line 61, Glenn discloses the following:

A semiconductor package 10 comprising: a substrate 11 comprising a plurality of bonding sites; a semiconductor die 24 on the substrate comprising a plurality of bond pads 25 in electrical communication with the bonding sites; a plurality of external contacts 20 on the bonding sites, each external contact comprising a "first metal layer" on a bonding site, a second metal layer "intermediate layer" on the first metal layer, and an inherently non-oxidizing outer layer "top layer of gold" on the second metal layer; and an encapsulant 28 on the substrate encapsulating the die; a plurality of die contacts 18 on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded (at least indirectly) to the bond pads on the die; a plurality of die contacts 18 on the substrate in electrical communication with the external contacts, and wherein the die is back bonded to the substrate and wire 26 bonded (at least indirectly) to the die contacts; wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold; wherein the die is wire bonded to the substrate in a chip-on-board configuration; wherein the die is wire bonded to the substrate in a board-on-chip configuration (the board is on the chip); wherein the substrate includes a recess 22 and the die is contained in the recess in contact with a heat spreader 11 (11 inherently spreads heat).

A semiconductor package comprising: a substrate comprising a board material; a plurality of die contacts on the substrate and a plurality of external contacts on the substrate in electrical communication with the die contacts, each die contact and each external contact comprising a base metal layer "first metal layer," a bump metal layer "intermediate layer" and a non-oxidizing outer metal layer "top layer of gold"; and a semiconductor die 62 flip chip mounted to the substrate, the die comprising a plurality of bond pads bonded to the die contacts; an encapsulant 68 on the substrate encapsulating the die; wherein the base metal layer comprises copper, the bump metal layer comprises nickel, and the non-oxidizing outer metal layer comprises gold; wherein each die contact and each external contact is generally pyramidal in shape "provided with a small negative draft" with a planar tip portion 36, 38, respectively.

A semiconductor package comprising: a substrate having a first side and an opposing second side; a plurality of die contacts on the first side comprising first multi layered metal bumps having generally planar first tip portions; a plurality of external contacts on the second side in electrical communication with the die contacts comprising second multi layered metal bumps having generally planar second tip portions; and a semiconductor die flip chip mounted to the substrate, the die comprising a plurality of bond pads bonded to the die contacts; wherein each first multi layered metal

bump and each second multi layered metal bump comprises a copper layer, a nickel layer and a gold layer; an encapsulant on the substrate encapsulating the die; wherein the die contacts have a pattern (at least a square pattern) matching that of the bond pads on the die and the external contacts are in a grid array.

A semiconductor package comprising: a substrate having a first side and an opposing second side; a plurality of die contacts on the first side; a plurality of bonding sites on the second side in electrical communication with the die contacts; plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and a semiconductor die back bonded to the first side in a chip-on-board configuration, the die comprising a plurality of bond pads wire bonded to the die contacts; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the non-oxidizing third metal layer comprises gold; an encapsulant on the substrate encapsulating the die.

A semiconductor package comprising: a substrate having a first side, an opposing second side and an opening 22; a plurality of bonding sites on the second side and a plurality of conductors 30 on the second side in electrical communication with the bonding sites; a plurality of external

contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and a semiconductor die bonded to the first side in a board-on-chip configuration, the die comprising a plurality of bond pads aligned with the opening and wire bonded to the conductors; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold; an encapsulant on the substrate encapsulating the die.

A semiconductor package comprising: a substrate having a first side, an opposing second side and a recess; a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites; a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; a heat spreader in the recess; and a semiconductor die in the recess in contact with the heat spreader, the die comprising a plurality of bond pads wire bonded to the conductors; an encapsulant in the recess encapsulating the die; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

An electronic assembly comprising: a supporting substrate 70 comprising a plurality of electrodes 76; at least one semiconductor package on the supporting substrate comprising: a substrate comprising a plurality of bonding sites; a semiconductor die on the substrate comprising a plurality of bond pads in electrical communication with the bonding sites; and a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer; wherein the substrate and the package are configured as a multi chip module; wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold; wherein the package further comprises a plurality of die contacts on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded to the bond pads on the die.

An electronic assembly comprising: a supporting substrate comprising a plurality of electrodes; and a semiconductor package comprising a substrate, a plurality of die contacts on the substrate comprising first multi layered metal bumps having generally planar first tip portions, a semiconductor die bonded to the die contacts in a flip chip configuration, and a plurality of external contacts on the substrate in electrical communication

with the die contacts comprising second multi layer metal bumps having generally planar second tip portions bonded to the electrodes; wherein each die contact comprise a copper layer, a nickel layer and a gold layer; wherein each external contact comprise a copper layer, a nickel layer and a gold layer.

To further clarify the disclosure of die contacts 18, bonded to the bond pads on the die, the term "die contacts" is a statement of intended use of the product that does not result in a structural difference between the claimed product and the product of Glenn. Further, because the product of Glenn has the same structure as the claimed product, it is inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed product from the product of Glenn. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re

Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Furthermore, as elucidated in the rejection, the contact 18, is at least indirectly bonded (contacted) to pads on the die.

Claims 5, 13, 21, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn as applied to claims 1, 9, 18, 22 and 26 supra, and further in combination with applicant's admitted prior art.

Glenn does not appear to explicitly disclose wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins; and a solder mask on the substrate configured to electrically insulate the external contacts.

Nevertheless, at page 2, lines 11-19; page 2, line 34 to page 4, line 11; and page 4, line 20 to page 5, line 24, applicant admits as prior art wherein the substrate 18 comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins; and a solder mask 34 on the substrate configured to electrically insulate the external contacts 26. Furthermore, it would have been obvious to combine

this prior art disclosure with the disclosure of Glenn because it would facilitate provision of the substrate and electrically insulate the contacts from each other.

Claims 1, 3, 4-8, 13, 18-29 and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (6122171) and applicant's admitted prior art.

At column 2, line 32 to column 3, line 6; column 4, lines 53-54 and 65-67; column 7, lines 47-60; and column 9, line 2, Akram discloses the following:

A semiconductor package comprising: a substrate 120/220, 242/320 comprising a plurality of bonding sites; a semiconductor die 112/212/312 on the substrate; a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer 158 on a bonding site, a second metal layer 154 on the first metal layer, and an inherently non-oxidizing outer layer 156 on the second metal layer; and an encapsulant 134 on the substrate encapsulating the die; a plurality of die contacts (location at intersection of substrate 320 and bond wires 332) on the substrate 320 in communication (at least indirect physical communication) with the external contacts, and wherein the die 312 is back bonded to the substrate and wire bonded to the die contacts; wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer

comprises gold; wherein the die 312 is wire 332 bonded to the substrate 320 in a chip-on-board configuration; wherein the die 112 is wire 132 bonded to the substrate 120 in a board-on-chip configuration; wherein the substrate 220/242 includes a recess (illustrated not labeled in FIG. 5) and the die is contained in the recess in contact with a heat spreader 243.

A semiconductor package comprising: a substrate 320 having a first side and an opposing second side; a plurality of die contacts on the first side; a plurality of bonding sites on the second side in communication with the die contacts; a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and a semiconductor die back bonded to the first side in a chip-on-board configuration, the die wire bonded to the die contacts; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the non-oxidizing third metal layer comprises gold; an encapsulant encapsulating the die; a substrate 120 having a first side, an opposing second side and an opening; a plurality of bonding sites on the second side and a plurality of conductors "traces" on the second side in electrical communication with the bonding sites; a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a

non-oxidizing third metal layer on the second metal layer; and a semiconductor die bonded to the first side in board-on-chip configuration, the die aligned with the opening and wire bonded to the conductors; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold; an encapsulant on the substrate encapsulating the die.

A semiconductor package comprising: a substrate 220, 242 having a first side, an opposing second side and a recess; a plurality of bonding sites on the second side; a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-
layer on the second metal layer; a heat spreader in the recess; and a semiconductor die in the recess in contact with the heat spreader, the die wire bonded to the substrate on the second side; an encapsulant in the recess encapsulating the die; wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

An electronic assembly comprising: a supporting substrate (bottommost 620) comprising a plurality of electrodes (illustrated not labeled in FIG. 6); at least one semiconductor package on the supporting substrate comprising: a substrate 620 comprising a plurality of bonding

sites; a semiconductor die 312 on the substrate in communication with the bonding sites; and a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer; wherein the substrate and the package are configured as a multi chip module; wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold; wherein the package further comprises a plurality of die contacts (illustrated not labeled in FIG 6.) on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded (at least indirectly) to the die.

However, Akram does not appear to explicitly disclose wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins; a solder mask on the substrate configured to electrically insulate the external contacts; the die comprising a plurality of bond pads in electrical communication with the bonding sites; the bond wires on the substrate in electrical communication with the external contacts; the bonding sites in electrical communication with the die contacts; a plurality of conductors in electrical communication

with the bonding sites, and the plurality of bond pads wire bonded to the conductors.

Nonetheless, at page 2, lines 11-19; page 2, line 34 to page 4, line 11; and page 4, line 20 to page 5, line 24, applicant admits as prior art; wherein the substrate 18 comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins; a solder mask 34 on the substrate configured to electrically insulate the external contacts 26; a die 14 comprising a plurality of bond pads 16 in electrical communication with the bonding sites 30; the bond wires 24 on the substrate in electrical communication with the external contacts 26; the bonding sites 30 in electrical communication with the die contacts 22; a plurality of conductors 22 in electrical communication with the bonding sites, and the plurality of bond pads wire bonded to the conductors. Moreover, it would have been obvious to combine this prior art disclosure with the disclosure of Akram because it would, facilitate electrical connection and provision of the substrate, and electrically insulate the contacts from each other.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

For information on the status of this application applicant should check PAIR:

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
2-Sep-04